REMARKS

This is in response to the Office Action dated July 11, 2003. Non-elected claims 1-15 have been canceled, without prejudice in view of the Restriction Requirement. New claims 17-23 have been added. Thus, claims 16-23 are now pending.

The title has been amended as suggested by the Examiner.

For purposes of example, and without limitation, certain example embodiments of this invention relate to a semiconductor device having a structure which allows for easier processing and alignment during the manufacture thereof. For example, Fig. 1 of the instant application illustrate a semiconductor device including *metal* gate electrode 19, gate insulator 13, respective *metal* contact plugs 20 provided over S/D regions 15, and interlayer insulator 22 provided over both the gate electrode 19 and isolation regions 12 (e.g., see especially Figs. 1(f) – 1(j)). The gate electrode 19 is electrically isolated from the contact plugs 20 by the sidewall insulating film(s) 16, and the gate electrode 19 and the contact plugs 20 both have the same height as best shown in Fig. 1(i). *Since the gate electrode 19 and contact plugs 20 are both formed of metal, they advantageously may both be formed in the same process step using the same material.* This unique structure is advantageous in that it allows an easier process of manufacture as explained above and also permits contact plugs 20 to be formed in the vicinity of the gate electrode 19 in a self-aligned manner, so that electrical isolation between the gate electrode 19 and contact plugs 20 is ensured for prevention of a short between the gate electrode and the contacts of the interconnection (e.g., pgs. 24-25). Further, the contact plugs 20 can be spaced by a

minimum distance from the gate electrode 19 as desired by adjusting the thickness of the sidewall insulating film 16. Therefore, the contacts can be provided close to the gate electrode, whereby a parasitic resistance in the source/drain regions can be reduced for improvement of the device characteristics of the transistor (e.g., pg. 25).

Claim 16

Claim 16 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Tseng. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 16 requires that both the gate electrode and the contact plugs are formed of metal(s) and that they have the same height. For example, see Fig. 1(i) of the instant application which illustrates metal gate electrode 19 and metal contact plugs 20 both having the same height. Forming both the gate electrode 19 and contact plugs 20 of metal is highly advantageous, for example, since this permits both the gate electrode and the plugs to be formed in the same process step of the same material, thereby simplifying the process of manufacture for the device.

In contrast with claim 16, Tseng's polysilicon gate electrode 106 does not have the "same height" as the alleged contact plug 122. Moreover, it cannot be said that Tseng's silicide layer 124 is the gate electrode since claim 16 clearly requires that the gate electrode be formed of metal. Thus, since claim 16 clearly require that the gate electrode be metal, it cannot be argued that silicide 124 makes up part of the gate – it does not according to the clear language of claim 16.

Furthermore, Tseng also fails to disclose or suggest metal contact plugs as required by claim 16. Instead, Tseng teaches directly away from this aspect of claim 16 by using silicide for alleged plugs 122 (silicide is not metal, as will be appreciated by those skilled in the art). For this additional reason, it can be seen that Tseng is entirely unrelated to the invention of claim 16.

Claim 17

Claim 17 requires that "an insulating film is provided over both the metal gate electrode and isolation regions on opposite sides of the gate electrode, but is not provided over at least part of the source/drain regions." For example, see Fig. 1(j) of the instant application which illustrates that insulating film 18, 22 is provided over both the metal gate electrode 19 and isolation regions 12 on opposite sides of the gate electrode, but is *not* provided over at least part of the source/drain regions 15. Clearly, Tseng fails to disclose or suggest this aspect of claim 17.

Claim 19

Claim 19 requires that "no silicide layer is provided over the gate electrode." For example, Fig. 1(j) of the instant application illustrates that no silicide layer is provided over the gate electrode 19. Again, Tseng fails to disclose or suggest this aspect of claim 19. Instead, Tseng teaches directly away from the invention of claim 19 since Tseng requires a silicide 124 over the gate 106.

Claim 20

Claim 20 requires that "conductive interconnects are provided over the respective contact plugs, and wherein at least portions of the interconnects are in contact with respective vertically aligned sidewalls of the contact plugs." For example, Figs. 1(i)-1(j) of the instant application illustrates that conductive interconnects 27 are provided over the respective contact plugs 20, wherein at least portions of the interconnects 27 are in contact with respective vertically aligned sidewalls of the contact plugs 20.

Claim 22

Claim 22 requires "a conductive interconnection (27) formed by a dual damascene process located over and contacting at least one of the contact plugs." Again, Tseng fails to disclose or suggest this aspect of claim 22.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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